AN429

Using the DC-DC Converter on the F9xx Series MCU for Single Battery Operation with the EZRadioPRO® RF Devices

1. Introduction

This application note explains how to configure the C8051F9xx's dc-dc converter in the one-cell mode to power the EZRadioPRO® device. In addition, this application note qualifies the effects on the RF performance due to the spurs generated by the dc-dc converter's switch frequency.

2. DC-DC Converter

The C8051F9xx series MCU devices include an on-chip dc-dc converter allowing for operation from a single cell battery with a supply voltage as low as 0.9 V. The dc-dc converter uses a switching boost converter with an input voltage range of 0.9 to 1.8 V, it also provides for a programmable output voltage range of 1.8 to 3.3 V (SFR register DC0CN). The default output voltage is 1.9 V.

The input voltage must be at least 0.2 V lower than the output voltage. The dc-dc converter can supply the system with up to 65 mW of regulated power and can be used for powering the radio and other devices in a given system.

Note: The dc-dc converter can safely provide up to 100 mW of output power without any risk of damage to the MCU, but unwanted VBAT and VDD/DC+ supply monitor resets are more likely to occur if the dc-dc converter provides more than 65 mW, in addition, higher output ripples, analog noise and less robust regulation may occur.

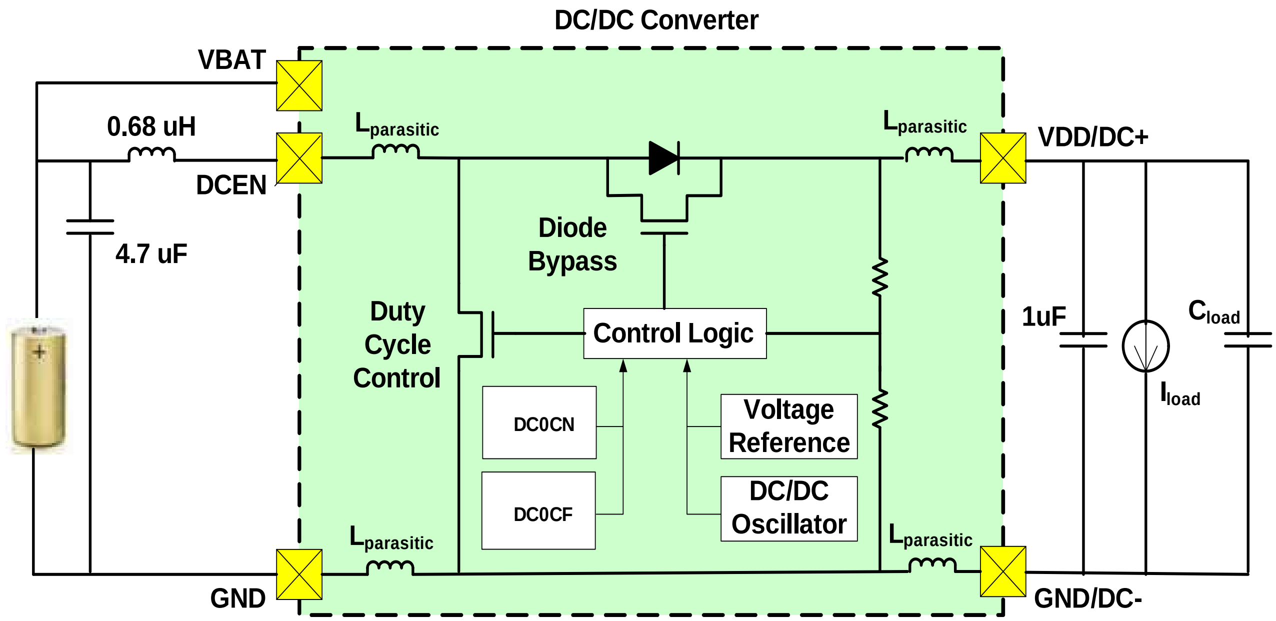

Figure 1. DC-DC Converter Block Diagram

In order to minimize noise on the power supply lines, GND and GND/DC– pins should be kept separate, as shown in Figure 1 and only one of them should be connected to the PCB ground plane.

In applications where the dc-dc converter is used to power only the MCU's internal circuits, then either the GND or GND/DC– may be used for the PCB ground. It is however recommended that in applications where the dc-dc converter is used to power external analog circuitry then the use of the GND/DC– be used for this purpose, the battery's negative terminal should not connected to board's ground.

For more detailed information on the C8051F9xx's dc-dc converter, refer to the C8051F9xx data sheet.

2.1. Enable the DC-DC Converter—One-Cell Mode

On a power-on reset, the state of the DCEN pin is sampled to determine if the MCU will power up in the one-cell or two-cell mode. In the two-cell mode, the dc-dc converter remains disabled. In one-cell mode, the dc-dc converter remains disabled only when in the sleep mode, in all other power modes the dc-dc converter will remain enabled.

The dc-dc converter is configured to operate in one-cell or two-cell modes through a hardware configuration. The one-cell mode is enabled (dc-dc converter enabled) by placing a 0.68 µH inductor between DCEN and VBAT. The two cell mode is enabled (dc-dc converter disabled) by shorting DCEN directly to GND. The DCEN pin should never be left floating. The device can only switch between one-cell and two-cell mode during a power-on reset.

When the dc-dc converter is enabled (one-cell mode), the following guidelines apply:

- GND/DC– pin should not be externally connected to GND.
- The 0.68 µH inductor should be placed as close as possible to the DCEN pin for maximum efficiency.
- The 4.7 µF capacitor should be placed as close as possible to the inductor.
- The current loop including GND, 4.7 µF capacitor, 0.68 µH inductor and the DCEN pin should be made as short as possible.
- The PCB traces connecting VDD/DC+ to the output capacitor and the output capacitor to GND/DC– should be as short and as thick as possible in order to minimize parasitic inductance.

2.2. DC-DC Converter Clocking

The dc-dc converter may be clocked using its internal oscillator, or from any system clock source, selectable by the CLKSEL bit (SFR register DC0CF). The dc-dc converter’s internal oscillator frequency is approximately 2.4 MHz. A more accurate clock source may be provided by a system clock, or a divided version of the system clock if required as the dc-dc converter has a built in clock divider (configured using DC0CF[6:5]) which allows any system clock frequency over 1.6 MHz to generate a valid clock in the range of 1.6 to 3.2 MHz.

3. Measurement Test Setup

The measurement test setup can be seen in Figure 2. In this configuration, an external power supply is used to ramp the supply from 0.9 to 1.8 V (one-cell mode) in order to measure the VDD/DC+ (DC-DC converter output) which will supply the RF device.

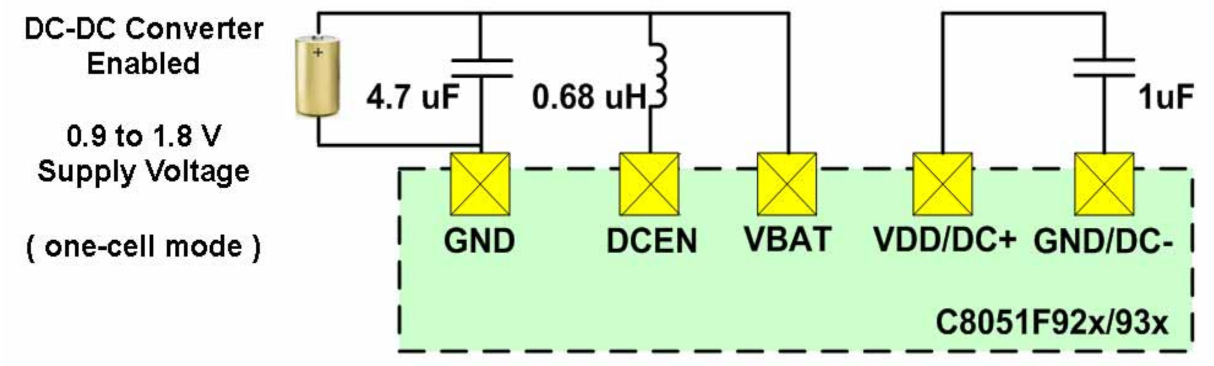

Figure 2. One-Cell Mode Connection

The MCU should then be programmed to use one-cell mode through the SFR DC0CN and DC0CF register. The configurations are shown below:

DC0CN:

- No minimum duty cycle
- Large dc-dc converter switch
- ADC0 Synchronization enabled
- DC-DC output voltage from 1.8 to 3.3 V

DC0FN:

- DC-DC clock divider (4) for the converter’s system clock source (8 MHz)
- DC-DC converter clock not inverted
- Peak inductor current limit max at 500 mA
- VDD-DC+ if float in sleep mode
- DC-DC converter clock source using system clock

3.1. Operation

- **Supply Line**: VBAT supply is ramped to a minimum of 0.9 V, this is used to supply the MCU after which the dc-dc converter will start up. Once the dc-dc converter has started, measure the VDD/DC+ line (supply source to the RF device) to ensure the desired pre-programmed voltage is available.
- **DC-DC Converter Clock**: Vary the converter clock speed (for the internal asynchronous 2.4 MHz and/or any external system clock) within the valid dc-dc converter clock range of 1.6 to 3.2 MHz to verify the presence of any spur generated on a spectrum analyzer.
  - A continuous wave (CW) signal is sent from the RF device.
  - A modulated OOK signal is sent from the RF device to qualify the transient behavior of the DC-DC converter to support the ramping of the PA for OOK modulation.

3.2. Measurements

- Verify VDD/DC+ supply generated by the dc-dc converter before transmit.
- Verify VDD/DC+ supply generated by the dc-dc converter when a CW/OOK signal is transmited.
- Capture the ringing effects of the external supply source and the VDD/DC+ source.
- Adjust the spectrum analyzer RBW and Span to check for adverse effects of the spur generated by the dc-dc converter and measure spur relative to the carrier signal.

4. Signals and Results

Figure 3. Signal 1, DC Signal at 1 V/div of VDD/DC+ Voltage Generated by DC-DC Converter Signal 2, AC Signal at 200 mV/div is Ringing on the VDD/DC+ (RF Supply Line)

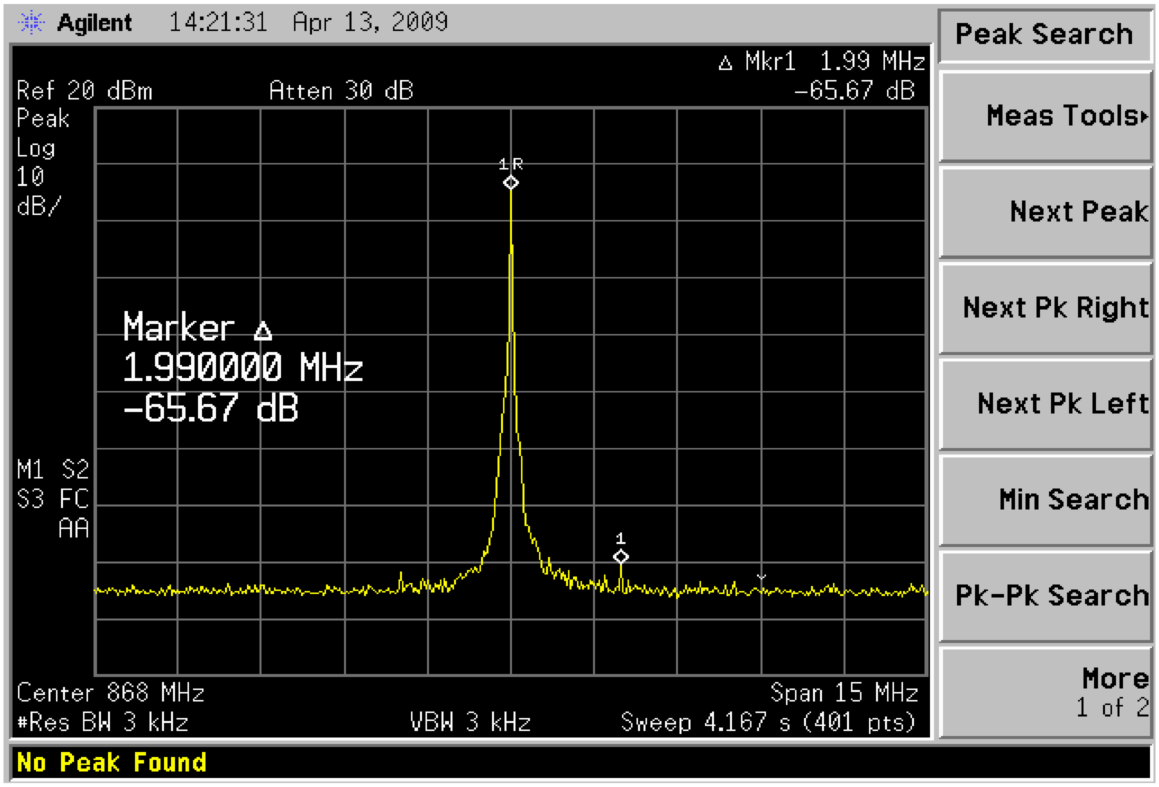

Figure 4. Spur Caused by DC-DC Converter (Does Not Violate ETSI or FCC Regulations)

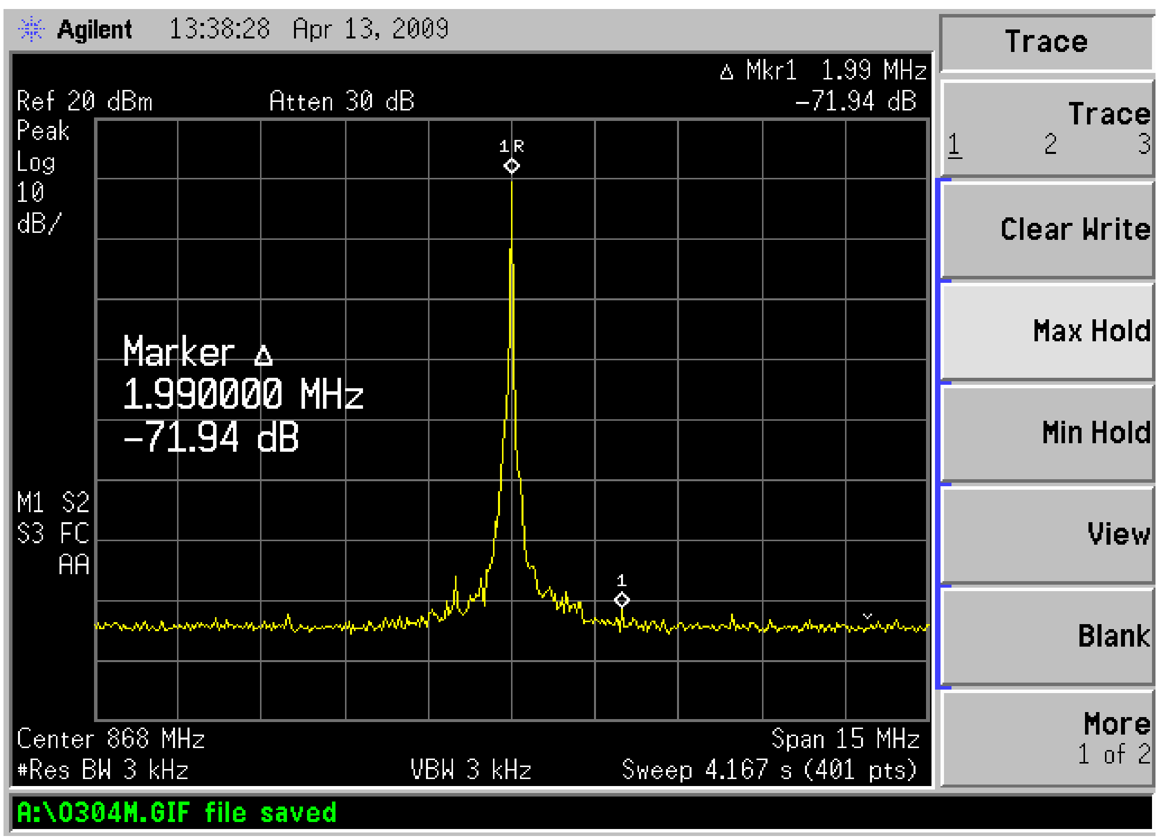

Figure 5. OOK Signal—Spur Measurement Relative to Carrier (Does Not Violate ETSI or FCC Regulations)

Measured data based on the following:

Device: Si4431-A0

Center Frequency: 868 MHz

Modulation: Continuous Wave (CW) GFSK modulation

Resolution Bandwidth used: 3 kHz

Table 1. Raw Data of the Spur Measurement Generated from the F9xx DC-DC Converter Relative to the Carrier of a Si4431-A0 Unmodulated GFSK Signal

Programmed DC-DC V	Input (V)	DC V (during CW)	DC-DC clock (MHz)	RF current (mA)	Spur (relative to carrier)
3.0	0.98	2.919	2.4	31.83	–69.0 dBc @ 2.4 MHz
	0.98	2.755	2	31.22	–66.25 dBc @ 2 MHz
2.4	0.98	2.385	2.4	29.84	–69.32 dBc @ 2.4 MHz
	0.98	2.385	2	29.85	–65.73 dBc @ 2 MHz
2.0	0.98	1.982	2.4	28.12	–68.76 dBc @ 2.4 MHz
	0.99	1.981	2	28.14	–68.66 dBc @ 2 MHz

5. Conclusion

The C8051F9xx internal dc-dc converter can supply the system up to a maximum of 100 mW. For the purposes of this app note, Silicon Labs results were based upon the Si4431-A0 device. In addition, since the dc-dc converter is optimized when running at a system clock of 1.6 to 3.2 MHz, the output supply line (VDD/DC+) was able to support both the RF CW or the OOK transmissions with ease and the spurs are typically in the –65 dBc range when the dc-dc converter clock was programmed to run within this range.

When running the C80519xx internal dc-dc converter from a system clock of 1.6 to 3.2 MHz, the output supply line (VDD/DC+) is able to support both RFCW or OOK transmissions with ease. The spurious effects of the dc-dc were typically –65 dBc when the dc-dc was operated with a system clock in the designed range.

The C80519XX + Si4431 is the only MCU+RF device available that can operate with a single-cell 1 V battery. There are no adverse effects on the RF performance while utilizing this power saving combination, and the RF performance can still easily meet the ETSI and FCC spurious requirements of –54 dBc.

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